500.35516CX1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Y. AKIBA et al

Serial No.: 09/956,909

Filed: September 21, 2001

For: LOW-EMI ELECTRONIC APPARATUS, LOW-EMI CIRCUIT BOARD, AND METHOD OF MANUFACTURING THE LOW-EMI CIRCUIT BOARD

Group: 2827

Examiner: T. DINH

RESPONSE TO NON-FINAL OFFICE ACTION

Commissioner For Patents
Washington, D. C. 20231

March 5, 2003

Sir:

In response to the outstanding Office Action, dated November 5, 2002, the period of response for which extension of time is requested in the attached Petition for Extension of Time, the following rebuttal discussion/arguments to the issues presently outstanding are respectfully submitted in connection with the above-identified application. (An authorized credit card payment form covering the fee amount for the extended time period is enclosed herewith.)

Responsive Discussion/Rebuttal Arguments

Claims 1-16 remain pending of which claims 3-13, 15 and 16 were earlier withdrawn. A non-final action on the merits was given with regard to claims 1, 2 and 14, in which the present response is directed thereto. Claims 1, 2 and 14 were rejected both on obviousness grounds, under 35 USC §103(a), as well as on "non-statutory" double patenting grounds. The discussion which follows is directed thereto.

As to the rejection under 35 USC §103(a), such as detailed under item 5, on pages 4-5 of the outstanding Office Action, the basis thereof is over the combination of Howard et al (US 5,708,569) in view of Johnson (US 4,179,797). It will be shown, hereinbelow, the invention according to claims 1-2 and 14 could not have been achievable such as alleged in the outstanding rejection. Accordingly, this rejection is traversed and reconsideration and withdrawal of the same is respectfully requested.

The invention is directed to a structure such as in connection with an electronic apparatus which suppresses spurious radiation by the circuit board when mounted on the electronic apparatus. A construction for attaining this is featured in connection with base claim 1 and, more particularly, with regard to the dependent claims 2 and 14 thereof. The present invention particularly relates to electronic devices which can cope with EMC and with regard to the manufacture of such a device, circuit board and an electronic apparatus which are facilitated with such spurious radiation or suppression capability.

The scheme called for in base claim 1 can be seen with regard to example embodiments such as shown in Figs. 2 and 7 of the drawings, although not limited thereto. With regard to the Fig. 2 example embodiment, ground

layers 3(G_1) and 5(G_2) and power layer 2 (V) relate to the first, second and third conductor layers, respectively, and, moreover, the dielectric insulators 14 and 15 relate to the first and second dielectric material layers while resistor material 6-1 and 6-2 in Fig. 2 relate to the "resistor layer" according to claim 1. Correspondingly, ground conductor layers 37(G_1) and 39(G_2) and power layer 36 (V) likewise relate to the claimed first through third conductor layers, respectively, and 38 and 40 relate to the first and second dielectric material layers while 41-1 and 41-2 relate to the resistor layer according to claim 1, respectively. As can be seen from these example embodiments, in Figs. 2 and 7 of the drawings, the second dielectric material layer (e.g., 15 in Fig. 2, and 40 in Fig. 7) is sandwiched by the third conductor layer (e.g., power layer V or layer 2 in Fig. 2 or layer 36 in Fig. 7) and the second conductor layer (e.g., ground layer (G_2), which is 5 in Fig 2 and 39 in Fig. 7). It is also seen, from the Figs. 2 and 7 illustrations, that the "resistor layer" (6-1, 6-2 in Fig. 2 and 41-1 and 41-2 in Fig. 7) is sandwiched by the first and second conductor layers and is connected electrically to the first conductor layer (3 in Fig. 2 and 37 in Fig. 7) and to the second conductor layer (e.g., 5 in Fig. 2 and 39 in Fig. 7). It is submitted, such a scheme as that called for in claims 1, 2 and 14 could not have been suggested from the combined teachings of Howard et al and Johnson.

Howard et al disclosed a circuit component assembly and method therefor which features a laminate construction such as shown with regard to Figs. 1-4 thereof. Such a construction, it is observed, includes a resistor assembly having resistor layers such as 36A, 36B and 36C that are formed in the same layer as that of the conductive layer in connection with effecting a desired circuit equivalent thereto. (Column 12, lines 47-49, in Howard et al.)

Johnson also disclosed a scheme for fabricating a resistor (resistor assembly), namely, a resistor array. According to Johnson's disclosure, the method of fabricating the resistor arrangement is comprised of the steps of (i) forming the plurality of the gaps in the board made of non-conductive material; (ii) filling the gaps with the insulation material (electrical resistance material) which is able to flow therein; and (iii) hardening the insulation material to effectuate a resistor within the board. It will be shown, hereinbelow, due to the differences in structure and intentions associated with the schemes taught by Howard et al and Johnson, the present invention could not have been realized therefrom.

It is alleged, in the standing rejection based on the combined teachings of Howard et al and Johnson, that the invention according to claims 1, 2 and 14 was obvious in view of their combined teachings. Namely, it is alleged that " [i] T would have been obvious ...to have a resistor material electrically connected to first and second conductor layers as taught by Johnson to employ the structure of Howard [et al] in order to provide interfacial continuity, minimum of impedance mismatch, and minimum of insertion losses." Regarding the featured aspects according to the details of dependent claim 2, moreover, the rejection alleges that "Howard discloses the structures shown in Figs. 1-4 wherein the first, second, and third conductor layers (22, 28 and 24) made by conductor foils [are] capable of being used as ground and power planes." Notwithstanding such assertions, the invention, according to claims 1, 2 and 14, as will be shown hereinbelow, is a clear and patentable improvement even over the combined teachings of Howard et al and Johnson.

Howard et al, it is noted, disclosed a scheme in which the resistor layer

(e.g., 36A, 36B, 36C) is provided in respective conductive layers, such as discussed above. It is also acknowledged, in the outstanding rejection, that Howard et al "did" not disclose that featured aspect, according to claim 1, which calls for the resistor layer to be connected electrically to the first and second conductor layers.

According to the teachings of Johnson's disclosure, the substrate 12, as shown in Figs. 1-5 thereof, does feature resistor material which is electrically connected to the first and second conductor layers such as resistance material 14 which effects electrical connection to the conductive layer 24 as well as to the conductive layer 28. However, according to Howard et al's scheme, in order to attain an equivalent circuit, the through-hole is provided within the PCB (printed circuit board) and the resistor is disposed in the same conductor layer. Based on this, it can be said that Howard et al neither disclosed nor suggested a scheme which would permit filling through-holes with the resistor material such as that taught by Johnson.

Johnson disclosed a scheme for fabricating only a minute resistor assembly, in which the through-hole is filled with resistor material (e.g., 14). It is clearly apparent, therefore, that both the purpose and construction of the scheme taught by Howard et al are quite different from that taught by Johnson. Moreover, there is no teaching therefrom that would have suggested modifying a scheme taught by Howard et al in the manner taught by Johnson. In fact, if Johnson's teachings were to have been combined with that of Howard et al in a manner such that the through-hole according to Howard et al is filled with the resistor material in the manner taught by Johnson, the desired results of Howard et al's scheme could not have been attainable.

For these and other reasons, it is, practically, impossible to effectuate the combination of Howard et al's teachings with that of Johnson in connection with realizing the present invention.

If one of ordinary skill would have sought to combine the teachings of Howard et al and Johnson, it is apparent that the equivalent circuit realized would be clearly different from that according to the present invention. For one, it is noted that the equivalent circuit of the conductive layer/resistor layer scheme according to claim 1 is different from the equivalent circuits disclosed by Howard et al and Johnson. In order to see this more clearly, enclosed herewith is an attached sheet including Sketches A and B, which show a conductive layer/resistor layer construction according to base claim 1 as well as an equivalent circuit thereof including the desired low Q effect.

Firstly, according to the Howard et al's disclosure, the resistor is formed in the same layer as that of the conductor layer in connection with the formation of the various equivalent circuits associated therewith (e.g., Figs. 9-12 thereof). According to Johnson's disclosure, the hole (e.g., 10) is formed in the insulator (e.g., 12) of the substrate. The resistor (e.g., 14, 20A, 20B, 20C) is injected into the hole to form only the resistor element between the internal layers, which is in clear contradistinction with that according to Howard et al's scheme. Accordingly, not only are the teachings of Howard et al and Johnson not combinable, insofar as the present claimed subject matter is concerned, but, moreover, there is no disclosure or suggestion of why one of ordinary skill would have even have attempted to combine Howard et al with that of Johnson.

For one, according to the present invention, the resistor layer is arranged in the internal layer and not in the same layer as the other conductor layer, as

can be seen from attached Sketch A, which is consistent with the example embodiments shown in Figs. 2 and 7 of the drawings, although not limited thereto. This is a clear difference from that taught by Howard et al. Moreover, according to the present invention, between the first and second conductor layers, in which the resistor layer is sandwiched therebetween, an additional, third conductor layer is formed (see Sketch A and conductive layer 2 in Fig. 2 as well as conductive layer 36 in Fig. 7). Such construction is clearly different from that taught by Johnson.

Secondly, the equivalent circuit realized from the example construction scheme according to claim 1 (see Sketch B) is, it is submitted, clearly different from the equivalent circuits realized with regard to both Howard et al and Johnson. As can be seen from Sketch B, one of the purposes of the present invention is to realize a low Q between the electric voltage source and ground. Noting this, the effect attained by the structural scheme according to claims 1, 2 and 14 or the equivalent circuit thereof is fundamentally different from that realizable even over the combined teachings of Howard et al and Johnson. That is, the schemes taught by both Howard et al as well as Johnson could not have led to a circuit equivalent scheme and the low Q effect realized by a construction such as according to claims 1 and 2 noting that the equivalent circuits thereof are quite different from that called for by the present invention. That is, even if one of ordinary skill would have sought to combine the teachings of Howard et al and Johnson, the structure realized would not have led an equivalent circuit as that according to the present invention. It is submitted, therefore, that the low Q realized between the electric voltage source and ground as well as the effective EMC suppression of the board itself, which are attainable according to the

present invention, could not have been attained from the combined teachings of Howard et al and Johnson. Such an EMC suppression like that which is realizable according to the present invention could not have been attained even from the combined teachings of Howard et al and Johnson because of the differences in the layered constructions.

According to claim 2, the first and second conductor layers are ground layers, respectively, while the third conductor layer is a power source layer. According to the outstanding rejection, it is alleged that this is taught from Figs. 1-4 in Howard et al. However, the invention according to claim 2 also stipulates that the resistor layer is disposed between the first conductor layer and a second conductor layer and as can be seen from the example in Fig. 2 and attached Sketch A, it is located in the peripheral portion of the first conductor layer. By employing such a construction, it becomes possible to suppress the spurious radiation from the substrate.

With regard to Howard et al's disclosure, the resistor is disposed in the same layer as the conductor layer. That is, the resistor is not disposed between the first conductor layer and the second conductor layer as that called for in claim 1. Moreover, the resistor is not disposed on the surface and in the periphery of the first conductor layer. It is clearly apparent, therefor, that like claim 1, the invention according to claim 2 is also considerably different from that taught by Howard et al. Also, for the same and similar reasons as that presented hereinabove, the invention according to claim 2 (as combined with base claim 1) also could not have been realized even in view of the combination of Howard et al with Johnson. Likewise, the invention according to dependent claim 14, it is submitted, is also patentable.

The second rejection presently outstanding involves a rejection on "non-statutory" double patenting grounds. Namely, claims 1-2 and 14 were rejected "under the judicially created doctrine of double patenting over claims 1-11, 16-19, and 21-24 of US Patent 6,353,540" (corresponding to the patented file of the prior, parent application of the present application). However, a review of the referred-to claims in the named U.S. Patent shows that there is a considerable difference from that of claims 1, 2 and 14 of the present application. For one, while the claim disclosure according to base claim 1 in the named U.S. Patent calls for a first dielectric material layer for joining the first conductor layer and the third conductor layer and also calls for a second dielectric material layer for joining the second conductor layer and the third conductor layer, the invention according to claim 1 is presented somewhat differently. Namely, according to claim 1, the first dielectric material layer is sandwiched by the second conductor layer and the third conductor layer and that the second dielectric material layer is sandwiched by the third conductor layer and the second conductor layer. Also, according to claim 1, the spacing between the first and third conductor layers and that between the third and second conductor layers does not preclude additional, for example, dielectric material from being disposed therebetween in which, also, the claimed first and second dielectric material layers may also necessarily be centrally disposed intervening dielectric material layers.

The resistor disclosed in claim 1 of the above-named U.S. Patent is set forth as joining the first conductor layer and second conductor layer while the resistor layer according to base claim 1 of the present application is set forth as being sandwiched by the first conductor layer and the second conductor layer and, moreover, the resistor layer being electrically connected to the first

conductor layer and the second conductor layer. It is noted that a number of other details of the claimed disclosure according to the above-named U.S. Patent are not necessarily detailed according to claims 1-2 and 14 of the present application. For these and other reasons, therefore, reconsideration and withdrawal of the standing "non-statutory" double patenting rejection is respectfully requested.

Therefore, in view of the responsive discussion/rebuttal arguments presented hereinabove, reconsideration as well as favorable action therefor on the present claimed subject matter and an early formal Notification of Allowability of the above-identified application is respectfully requested.

If the present response renders the present application allowable except for the presence of "non-statutory" double patenting concerns, the Examiner is urgently requested to telephone applicant's representative so that any such remaining issue can be further discussed for the purpose of resolving the same and thereby rendering the application in condition for formal allowability.

If the Examiner deems that additional questions and/or issues still remain which would prevent the present application from being allowed at the present time, he is urgently invited to telephone the undersigned representative, at the number indicated below, so that either a telephone or personal interview may be arranged at the Examiner's convenience in order to discuss the same and hopefully resolve any remaining questions/issues present.

To the extent necessary, applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees to the Deposit Account of

Antonelli, Terry, Stout & Kraus, LLP, Dep. Acct. No. 01-2135 (500.35516CX1),

and please credit any excess fees to such deposit account.

Respectfully submitted,
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